Enabling *P*-type Conduction in Bilayer 2D Semiconductors with Sputtered Topological Semimetal Contacts

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Two-dimensional (2D) semiconductors are promising for low-power complementary metal oxide semiconductor (CMOS) electronics, which require ultrathin *n*- and *p*-type transistors with good contacts. However, good contact resistance has not been achieved with industry-compatible contact deposition for either *n*- or *p*-type channels, and some materials (like WS_2) have not been found to have good *p*-type contacts at all, due to their 'deeper' valence band. Here, we report advances in both of these directions, by using sputter-deposited topological semimetal NbP as *p*-type contacts. On bilayer WS_2 and WSe_2, this approach yields up to 5.8 µA/µm and 164 µA/µm hole current, respectively, at room temperature. These are the highest to date for any sub-2 nm thin WS_2 and highest for WSe_2 with sputtered contacts. The *p*-type conduction is enabled by the simultaneously high work function and low density of states of NbP, which reduce Fermi level pinning. The NbP is sputter-deposited at room temperature, which is compatible with CMOS fabrication and a step towards enabling ultrathin 2D semiconductors in future nanoelectronics.

Computing in the 21st century must process increasingly complex data loads, with recent large language models estimated to use as much energy as a small city every day[1]. From the hardware side, reducing energy use could be addressed by three-dimensional (3D) integration of logic and memory with dense interconnects, an approach that could yield 100× or higher energy efficiency per function[2]. Dense 3D integration calls for materials stacked at sufficiently low temperatures to avoid damaging existing (memory or logic) layers[3,4], and low-power operation requires complementary metal oxide semiconductor (CMOS) technology, with both *n*- and *p*-type transistors[5,6]. Energy-efficient, 3D electronics could benefit from adopting two-dimensional (2D) semiconductors, in nanosheet transistors[7] or in back-end-of-line (BEOL) logic and memory layers, due to their favorable mobility in sub-2 nm thin films[8,9] and their compatibility with lower temperature fabrication[10,11] than crystalline silicon.

The adoption of 2D semiconductors in future electronics hinges, in great part, on finding approaches to contact them in an industry-compatible manner. Moreover, while contacts to 2D materials are commonly made using metal evaporation[12–14] or layer transfers[15,16], these methods are not compatible with industrial semiconductor manufacturing, which uses sputtered metal contacts[17,18]. In addition, *p*-type contacts have proven more difficult than *n*-type for 2D semiconductors, primarily because conventional contact metals cause metal- and defect-induced gap states (MIGS and DIGS) which pin the Fermi level unfavorably (**Fig. 1a**). Thus, the realization of *p*-type contacts to ultrathin 2D semiconductors remains a pressing challenge, particularly if it can be done through industry-compatible means.

Here we advance both of these key challenges with sputter-deposited topological semimetal NbP as *p*-type contacts to bilayer 2D semiconductors WS_2 and WSe_2. Such semimetal contacts are expected to have large work function based on density functional theory (DFT) calculations[19], and their low density of states near the Fermi level could limit Fermi level pinning, enabling improved hole injection (**Fig. 1b**). NbP is also a Weyl semimetal, previously found to show signatures of topological protection in single crystal[20] and ultrathin nanocrystalline films[21] similar to Bi_2Se_3[22]. When interfaced with bilayer WS_2 (or WSe_2), such topological semimetals could display suppressed MIGS, and their large work function better aligns the Fermi level with the bilayer WS_2 (or WSe_2) valence band (**Fig. 1b,c**, **Supplementary Fig. S1-3**), both desired features for *p*-type conduction.

On bilayer WS_2 and WSe_2 transistors, our approach yields up to 5.8 µA/µm and 164 µA/µm hole current, respectively, at room temperature and -1 V drain-source voltage. These are the highest currents to date for any sub-2 nm thin WS_2 and the highest for WSe_2 with sputtered, industry-compatible contacts. Our WS_2 hole currents are also ~50 times higher than previous results, due to the 'deeper' valence band of this material which has made *p*-type contacts more difficult. The NbP contacts were sputtered directly on WS_2 and WSe_2 at room temperature, a process compatible with 3D and BEOL integration[3], as well as large-scale manufacturing[17,18] (see **Methods** for details). NbP contacts sputtered on *monolayer* WS_2 were found to cause significant defects (see **Supplementary Fig. S3** and **S4a)**; thus, we focus primarily on *bilayer* WS_2 and WSe_2 in this study, which are less sensitive to process damage (**Supplementary Fig. S4b)** and have 'shallower' valence bands[23] than their monolayers (**Fig. 1c**).

To examine the interface of NbP contacts with bilayer WS_2, we performed high-resolution scanning transmission electron microscopy (STEM) across such a stack on SiO_2/Si (**Fig. 2a-c**), similar to the transistor contacts employed further below. Here, the bilayer WS_2 films were directly grown by chemical vapor deposition (CVD)[24] onto the SiO_2/Si substrate. STEM images show the conformal deposition of ~3.5 nm sputtered NbP onto bilayer WS_2 without obvious defects (**Fig. 2a**).

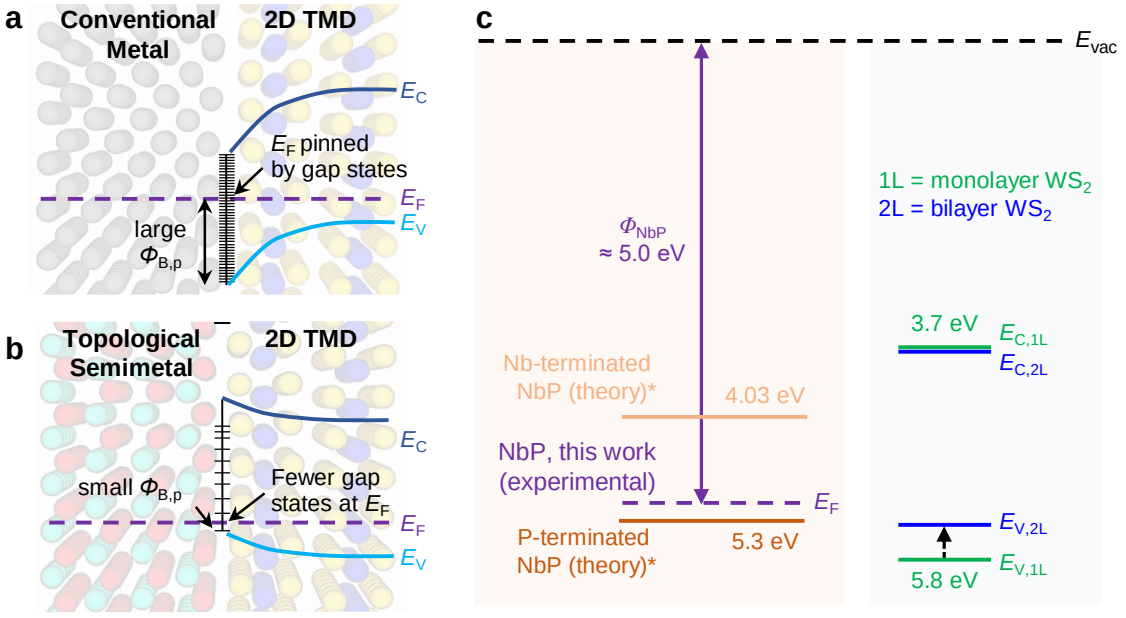

Figure 1 | Contacts to 2D transition metal dichalcogenides (TMDs). a, Conventional metal, and **b,** topological semimetal interfaced with a 2D TMD like WS_2 or WSe_2. The conventional metal tends to cause significant Fermi level (E_F) pinning in the band gap, leading to large Schottky barrier height for hole conduction ($\phi_{B,p} = E_F - E_V$). In contrast, topological semimetals with large work functions, such as NbP (and TaP), are expected to have less pinning and lower hole barrier height. E_C and E_V denote the conduction and valence band edges, respectively. **c,** Schematic diagram of NbP-WS_2 band alignments. The valence band of bilayer (2L) WS_2 is higher than that of monolayer (1L), and better aligned with our experimental work function of NbP (see **Supplementary Fig. S1** and **S2**). The expected work function of NbP (marked by *) and the WS_2 bands are based on Refs. 19,23,25.

The elemental energy dispersive spectra (EDS) in **Fig. 2d-h** confirm uniform distribution of Nb and P in our NbP film on bilayer WS_2. Atomic force microscope (AFM) mapping also reveals low surface roughness and continuous NbP both on SiO_2 **(Supplementary Fig. S5a**) and WS_2 (**Fig. 2i** and **Supplementary Fig. S5b**). Previous work has found that many metals deposited on 2D semiconductor surfaces tend to aggregate and form clusters[14,26]. However, our NbP deposited on WS_2 has no measurable change in surface roughness compared to when sputtered on SiO_2. Both top-down AFM and cross-sectional TEM imaging suggest intimate NbP-WS_2 contacts, without agglomeration. We also used Raman spectroscopy before and after NbP deposition, finding that the E_g and A_{1g} peaks of bilayer WS_2 (**Fig. 2j**) are essentially unaffected by the deposition of NbP (of either ~2 nm or ~3.5 nm thickness), unlike for monolayer WS_2 (**Supplementary Fig. S4a**). However, the formation of some defects is not unexpected[14,27] after direct sputtering of NbP on WS_2, as suggested by the increased LA(M) peak intensity[28] (**Supplementary Fig. S4b-d**), especially as the number of WS_2 layers is decreased.

We fabricated bilayer WS_2 transistors with NbP and TaP contacts (**Fig. 3a,b**), capped by Pd/Au, as well as control devices with only Pd/Au contacts. Devices have channel lengths L between 100 nm and 1 μm, channel widths of 1 or 2 μm, and are back-gated by the heavily doped Si substrate through

100 nm SiO_2. A top-down scanning electron microscope (SEM) image of a WS_2 bilayer 'strip' with multiple device channels is shown in **Fig. 3b**, and additional fabrication details are given in **Methods**.

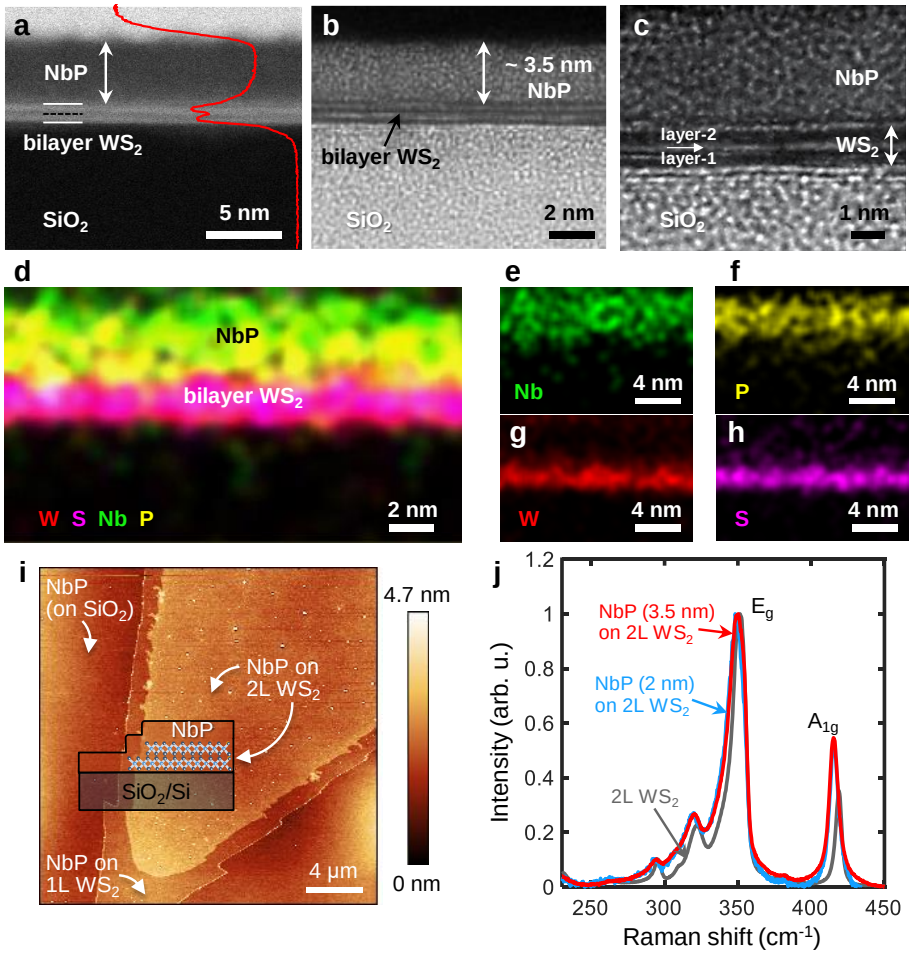

Figure 2 | Characterization of the NbP/bilayer WS_2 interface. a, High-angle annular dark field imaging (HAADF) scanning transmission electron microscopy (STEM) cross-section of NbP sputtered onto bilayer WS_2 on an SiO_2/Si substrate. STEM shows ~3.5 nm NbP film conformally deposited on the ~1.3 nm thin bilayer WS_2 (horizontal lines mark the edges of the layers and the van der Waals gap between them). **b,** Higher-resolution, and **c**, zoomed-in STEM images of the same sample. **d**, Energy dispersive spectroscopy (EDS) showing the elemental distribution of Nb, P, W, and S (combined), and of **e,** Nb, **f,** P, **g,** W, and **h,** S atoms (separately). The EDS measurement scan time was short to minimize electron-beam damage of the NbP/WS_2 stack and interface. This led to a lower-resolution EDS as a trade-off. **i,** Surface mapping with atomic force microscopy of ~3.5 nm NbP on bilayer WS_2 and nearby SiO_2 substrate, showing similar low surface roughness on both regions (~0.16 nm) (see **Supplementary Fig. 4**). Inset shows a cross-section schematic of the NbP covering steps of monolayer (1L) and bilayer (2L) WS_2. **j,** Raman spectra (532 nm laser, at room temperature) of bilayer WS_2 before (gray) and after (blue and red) being covered by NbP of two different thicknesses (~2 nm and ~3.5 nm), all showing similar E_g and A_{1g} peaks (normalized to the E_g peak intensity). The E_g and A_{1g} peaks correspond to in-plane and out-of-plane atomic vibrations, respectively.

Fig. 3c displays measured drain current vs. gate voltage (I_D vs V_{GS}) of bilayer WS_2 transistors, revealing >100× larger $|I_{D,max}|$ for our NbP-contact devices than our control Pd-contact devices. Similarly, our bilayer WS_2 devices with TaP contacts (another topological semimetal candidate) also show

enhanced *p*-type current compared to control Pd contacts (**Supplementary Fig. S6a**). When probing the positive V_{GS} range (**Supplementary Fig. S7**), Pd-contacted bilayer WS_2 devices also show stronger *n*-type behavior, similar to previous reports on ultrathin WS_2 using traditional metal contacts[13,28].

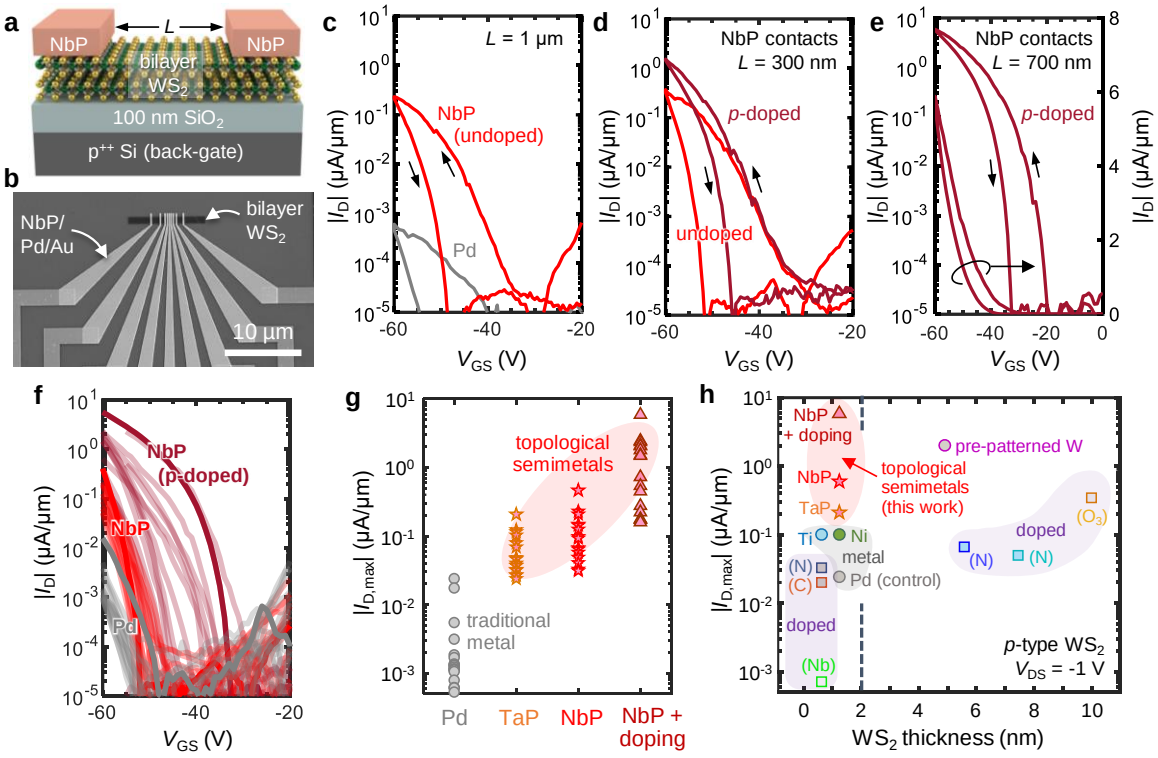

Figure 3 | Bilayer WS_2 transistors with NbP and TaP semimetal contacts. a, Schematic of a back-gated bilayer WS_2 transistor, not to scale. **b,** Top-view SEM image of fabricated devices with NbP contacts capped by Pd/Au. **c,** Measured I_D vs. V_{GS} at V_{DS} = -1 V for bilayer WS_2 transistors with NbP contacts (red) and Pd contacts (gray), at channel length L = 1 μm. Small arrows mark forward and backward sweeps[29], revealing similar hysteresis with both contact types. **d,** I_D vs. V_{GS} at V_{DS} = -1 V for a different bilayer WS_2 device (L = 300 nm) with NbP contacts before (red) and after (dark red) additional *p*-type doping, achieved by soaking the device in chloroform. **e,** I_D vs. V_{GS} at V_{DS} = -1 V showing maximum hole current of 5.8 μA/μm in another bilayer WS_2 device (L = 700 nm) with NbP semimetal contacts and additional *p*-doping. I_D is shown on both linear and log scale axes. **f,** Measured I_D vs. V_{GS} at V_{DS} = -1 V for 15 bilayer devices (each) with Pd contacts (gray), NbP contacts (red), and NbP contacts with additional doping (dark red). Darker color lines represent the highest-current device of each kind. **g,** Maximum *p*-type current $|I_{D,max}|$ achieved at V_{DS} = -1 V of devices with various contacts, including Pd, TaP (another topological semimetal), and NbP (before and after additional doping); 15 devices (symbols) are shown for each type. **h,** Benchmarking maximum *p*-type current $|I_{D,max}|$ vs. WS_2 (channel) thickness at V_{DS} = -1 V with various contact materials and doping strategies[30–37], including NbP and TaP semimetals, and control Pd metal from this work. (Text labels in parenthesis next to the symbols represent the doping type used.) Our results with NbP semimetal contacts enable the highest hole currents to date (up to 5.8 μA/μm) achieved in bilayer WS_2, >50× larger than previous reports with sub-2 nm channel thickness. All devices in panels **c-g** are between 1 and 2 μm wide, and the I_D reported is normalized (μA/μm) by the channel widths[29].

To further increase the hole current of our NbP-contacted bilayer WS_2 devices we applied chloroform doping[38,39] (see **Methods**). With this, we measured $|I_{D,max}|$ up to 5.8 μA/μm at V_{DS} = -1 V, nearly an order of magnitude higher than before doping, as shown in **Fig. 3d-f** and **Supplementary Fig. S8a,b**. The chloroform-doped devices also show a positive shift of threshold voltage, another signature

of *p*-type doping. We summarize the maximum hole current of various bilayer WS_2 devices using different contacts in **Fig. 3g** (15 devices for each contact type). Despite the device-to-device variability, much of it inherent to academic nanofabrication, we note a clear trend of enhanced *p*-type conduction with our semimetal contacts (TaP and NbP) vs. conventional Pd contacts. With NbP contacts and doping, the *p*-type current is increased by two orders of magnitude vs. Pd contacts to bilayer WS_2.

We also note that the observed hysteresis remains a challenge in *p*-type TMDs on SiO_2[40] (compared to *n*-type MoS_2), and is sometimes not reported. The hysteresis likely occurs due to the alignment of the TMD valence band with trap states in the SiO_2[41], due to interface adsorbates remaining from the TMD layer transfer process[42], and due to the imperfect nature of the as-grown materials today[43]. These drawbacks are not fundamental and are expected to be resolved as the quality of dielectrics, TMDs, and their interfaces improves. Nevertheless, fair device-to-device comparisons can be made when sufficient devices are measured and only the contacts are changed, as in **Fig. 3f,g**.

Using NbP and TaP semimetal contacts, we achieved the highest *p*-type currents to date in sub-2 nm thin WS_2 (**Fig. 3h**). Including doping, our devices reached ~5.8 µA/µm at V_{DS} = -1 V, over 50 times higher than previous reports in this WS_2 thickness regime. In contrast, traditional metal contacts like Ti[32], Ni[33], or our control Pd show much suppressed *p*-type behavior on ultrathin WS_2. Thicker WS_2 (e.g., ~5 nm) grown from pre-patterned tungsten contacts does show *p*-type conduction[35]; however, this thickness offers no electrostatic benefits over silicon in nanoscale transistors. **Fig. 3h** also displays additional data with traditional metal contacts to WS_2, where relatively low *p*-type currents were obtained after substitutional doping (using Nb[34], C[31], N[30,36]) or charge-transfer doping (e.g., WO_x[37]).

We note that the highest measured $|I_{D,max}|$ in our devices is limited by the largest $|V_{GS}|$ we can apply without compromising the back-gate dielectric integrity. In addition, the valence band of bilayer WS_2 is sufficiently 'deep' so as to render the threshold voltage quite negative here. This means that, even at our highest $|V_{GS}|$ = 60 V, not all our devices are fully turned on, especially not the Pd-contacted ones (**Fig. 3f**). Nevertheless, we can estimate an upper bound around 80 kΩ·µm for the *p*-type contact resistance of NbP to bilayer WS_2, as half the total resistance of the device with the highest current. Our estimated contact resistance to WS_2 is presently ~50 times lower than any previous results with this 2D semiconductor at sub-2 nm thickness (see **Supplementary Fig. S9**).

We also fabricated bilayer WSe_2 transistors with NbP contacts (capped by Pd/Au), using back-gated TLM structures similar to those in **Fig. 3a,b** followed by chloroform doping (see **Methods**). We choose WSe_2 not only to replicate the NbP contacts on another TMD channel, but also because it has

a 'shallower' valence band[19,25] (than WS_2) which has enabled more *p*-type demonstrations to date, although only with evaporated metal[44,45] or transferred contacts that are less compatible for industry scalability[15,16]. Devices have channel lengths L between 50 nm and 1 μm and additional fabrication details are given in **Methods**. **Fig. 4a** displays measured drain current vs. gate voltage (I_D vs V_{GS}) of two bilayer WSe_2 transistors, revealing up to 164 μA/μm at V_{DS} = -1 V for L = 70 nm. (We note that hysteresis in our WSe_2 is smaller than in our WS_2 devices, likely because the shallower valence band of WSe_2 overlaps with fewer SiO_2 trap states[41].) Electrical data for all 64 devices measured can be found in **Supplementary Fig. S10**. The maximum current $|I_{D,max}|$ vs. L is displayed in **Supplementary Fig. S11d**, showing repeatability and $I_{D,max}$ scaling with channel length.

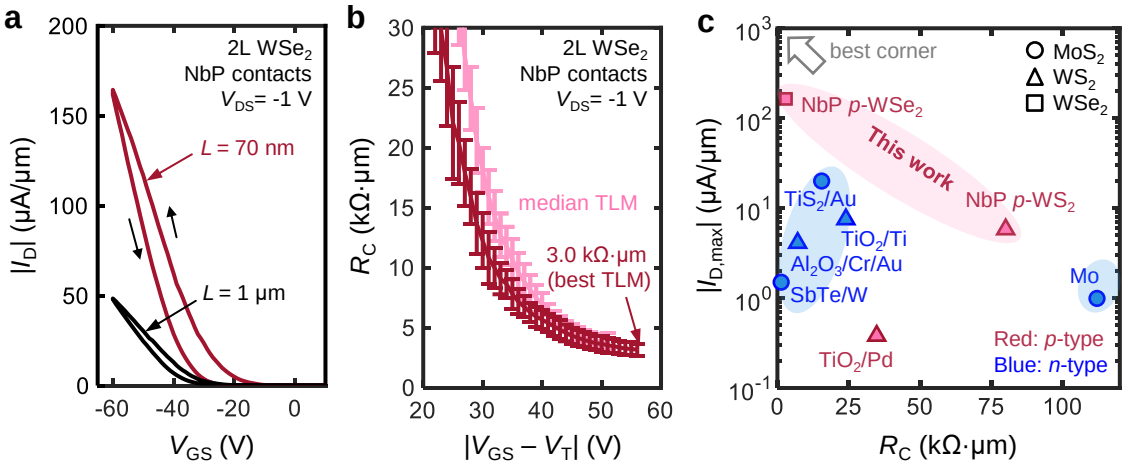

Figure 4 | Bilayer WSe_2 transistors with NbP semimetal contacts and doping. a, Measured I_D vs. V_{GS} at V_{DS} = -1 V for back-gated, bilayer WSe_2 with NbP contacts followed by chloroform doping at channel length L = 1 μm *and* L = 70 nm, reaching 164 μA/μm. Small arrows mark forward and backward sweeps[29]. **b**, Contact resistance (R_C) vs. gate voltage overdrive, $|V_{GS} - V_T|$, for NbP contacts to bilayer WSe_2, with R_C down to 3.0 kΩ·μm. Corresponding transfer length method (TLM) plots are shown in **Supplementary Fig. S11e**. **c**, Benchmarking devices which used industry-compatible contact deposition (sputtering[46,47] or atomic layer deposition[48–50]) for MoS_2 (○), WS_2 (Δ), and WSe_2 (□), all at $|V_{DS}|$ = 1 V. Red symbols mark *p*-type (hole) contacts, blue symbols mark *n*-type (electron) contacts. Our results with sputtered NbP contacts to bilayer WSe_2 (red □) enable the lowest R_C and highest I_D achieved to date with industry-compatible deposition among both *n*- and *p*-type TMDs. Our *p*-type NbP contacts to bilayer WS_2 (upper red Δ) represent the highest hole current achieved in this material to date. Top-left corner is most desirable in this plot (low R_C, high I_D).

From our TLM structures (**Supplementary Fig. S11e**), we estimate the contact resistance (R_C) in **Fig. 4b** as a function of overdrive voltage, $|V_{GS} - V_T|$. Our NbP-contacted bilayer WSe_2 has R_C as low as ~3.0 kΩ·μm at room temperature, which is the lowest hole contact resistance with sputtered contacts achieved on this material, to date. In **Fig. 4c** we benchmark both R_C and $|I_{D,max}|$ for contacts achieved with industry-compatible deposition techniques (sputtering or atomic layer deposition) to various TMDs. Few studies can be included here, because the vast majority of contacts to date have been made

with evaporated metals[44,45] or layer transfers[15,16]. Our sputtered NbP contacts to bilayer WSe_2 represent the lowest R_C and highest I_D to date with industry-compatible deposition among both *n*- and *p*-type TMDs[46–50]). Our NbP contacts to bilayer WS_2 are less effective (due to the 'deeper' valence band of this material[19,25]), but nevertheless reach ~50 times higher hole current than previous reports in this WS_2 thickness regime (also see **Fig. 3h**). Combined, these results are an existence proof that sputtered semimetal contacts could be engineered and optimized for TMDs in an industry-compatible fashion.

While obtaining good hole contacts to WSe_2 is perhaps less surprising, it remains of interest to understand what enables such behavior at NbP contacts with WS_2, which has a much 'deeper' valence band. To this end, we perform DFT simulations of the contact schematic in **Fig. 5a** using Quantum ESPRESSO[51], then extract the DOS and the hole Schottky barrier height $\phi_{B,p} = E_F - E_V$, as labeled on **Fig. 5b,c**. We estimate the density of metal-induced gap states (MIGS) by integrating the DOS across the band gap. The locations of WS_2 band edges are approximate, and further simulation details are given in the **Methods** section.

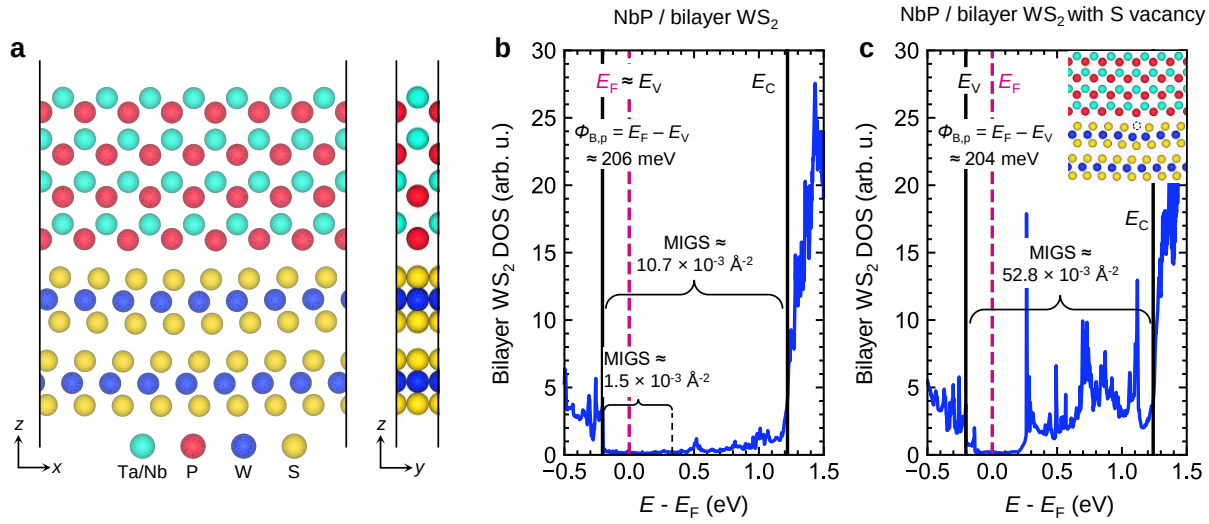

Figure 5 | Density Functional Theory (DFT) Simulations. a, Cross-section schematics of the DFT supercell for the semimetal contact (NbP or TaP) with bilayer WS_2. (Left) *x*-*z* cut and (right) *y*-*z* cut. **b**, Projected density of states (pDOS) contributions from bilayer WS_2 to the overall DOS of the NbP contact with bilayer WS_2. The hole Schottky barrier height ≈ 206 meV. **c**, pDOS for the same contact but with one S vacancy per unit cell (defect density of ~1.4×10^{14} cm^{-2}), displaying a nearly unchanged hole Schottky barrier height ≈ 204 meV. The inset displays the supercell with the sulfur vacancy marked by a black dotted line. In panels **b-c**, the Fermi energy E_F is referenced to zero and marked with a dashed purple line; the valence band maximum E_V and conduction band minimum E_C are marked with solid black lines. Locations of band extrema are estimated from projected band structures (see **Supplementary Section II**). MIGS densities are calculated by integrating the bilayer WS_2 pDOS across the denoted energy ranges.

In **Fig. 5b**, we estimate a small Schottky barrier ($\phi_{B,p} \approx 206$ meV) for the NbP contact with pristine bilayer WS_2 (i.e., without defects). This is comparable to the expected band alignment for an ideal

scenario without Fermi level pinning ($\phi_{B,p} \approx$ -100 meV, see **Supplementary Section I**). These results also suggest weak Fermi level pinning at the NbP/bilayer WS_2 interface because of the low MIGS densities formed, between ~1.5×10^{-3} Å^{-2} and 10.7×10^{-3} Å^{-2}, depending on the energy range of the DOS integral (the lower value being within 0.5 eV of E_V, where pinning states are more likely to play a role). We also simulate the bilayer WS_2 contact with TaP and find a hole barrier height of 138 meV, unlike the ideal pinning-free scenario of -200 meV (**Supplementary Fig. S12a**); however, experimentally we find TaP does not provide contacts as good as NbP to bilayer WS_2 (**Fig. 3g,h**), ostensibly due to greater damage during deposition. In contrast to these semimetals, our simulations for a conventional metal contact (W) on bilayer WS_2 reveal a large hole Schottky barrier ≈ 1 eV and large MIGS density (~57.7×10^{-3} Å^{-2} across the entire band gap or 11.3×10^{-3} Å^{-2} within 0.5 eV of E_V), as shown in **Supplementary Fig. S12b,c**. The estimated MIGS densities at our NbP/bilayer WS_2 contacts are also smaller than those of various conventional metal/2D semiconductor contacts from the literature[19,52].

We recall that direct deposition of semimetals or conventional metals[14,27] onto 2D semiconductors could create defects. To understand this, we perform additional DFT simulations (**Fig. 5c**) after introducing one sulfur (S) vacancy per unit cell in the top WS_2 layer, corresponding to a high defect density of ~1.4×10^{14} cm^{-2}. Even in this case, we estimate a nearly unchanged $\phi_{B,p} \approx$ 204 meV at our NbP contacts with bilayer WS_2, smaller than most metal-WS_2 systems[19,52]. Together, the favorable band alignment between NbP and bilayer WS_2, with sufficiently small MIGS densities (which prevent strong Fermi level pinning) support the favorable *p*-type conduction observed in our experiments with NbP contacts. Our calculations suggest a larger, non-negligible hole Schottky barrier for NbP with *monolayer* WS_2 ($\phi_{B,p} \approx$ 541 meV in **Supplementary Fig. S13**). This appears to occur due to the larger band gap and electron affinity (i.e., 'deeper' valence band) of monolayer WS_2 compared to bilayer WS_2.

In summary, we described sputtered topological semimetal *p*-type contacts to thin, bilayer WS_2 and WSe_2. NbP-contacted WS_2 transistors reach 5.8 µA/µm hole current, over 50 times larger than previous *p*-type WS_2 devices with sub-2 nm thickness. Bilayer WSe_2 devices reach up to 164 µA/µm hole current and 3.0 kΩ·µm contact resistance, the best to date for an industry-compatible deposition technique. The improved *p*-type behavior is enabled by the simultaneously large work function and low density of states of the NbP semimetal, leading to small hole barrier heights, further assisted by subsequent doping. Notably, the NbP was deposited by sputtering, one of the few demonstrations of industry-compatible contacts to 2D semiconductors. These results also provide physical insight into contact formation to the valence band of TMDs, and a possible route for their incorporation into future CMOS nanoelectronics.

METHODS:

Semimetal Deposition. We sputter deposited the NbP (and TaP) thin films at room temperature, an approach compatible with back-end-of-the-line (BEOL) semiconductor fabrication. Direct current (dc) magnetron sputtering was performed at a power of 12 W and pressure of 3 mTorr. The chamber base pressure was below 5×10^{-8} Torr. The distance between the sample and the sputtering target source was kept as large as possible (~9 inches) to minimize defect formation in WS_2 from the sputtering deposition. We note that compared to NbP, the compositional stoichiometry for TaP (1:1) was difficult to achieve during sputtering because of the heavier Ta vs. lighter Nb atoms. This also led to possibly greater damage of WS_2, causing TaP to not provide as good contacts as NbP to bilayer WS_2.

Raman Spectroscopy. Raman measurements were done using the Horiba Labram HR Evolution Raman system in the Stanford Nanofabrication Shared Facility. A 532 nm laser source with 1% laser power and spot size ~ 0.5 μm was used, which ensures minimal sample heating during measurement.

Transmission Electron Microscopy (TEM). Samples for TEM cross-section were fabricated by focused ion beam (FIB) milling (Helios NanoLab G3, FEI). To minimize ion milling damage, the final thinning was quickly performed using the 5 kV ion beam. Double spherical aberration (Cs) corrected TEM (Themis Z, ThermoFisher Scientific) with 80 pm resolution was used for the cross-section of bilayer WS_2 under NbP. To minimize the electron beam damage, the acceleration voltage was set to 80 kV and the screen current remained under 20 pA. In high angle annular dark field (HAADF) scanning TEM (STEM), a probe convergence angle of 20.5 mrad and the inner and outer collection semi angles of 108 mrad and 200 mrad were used, respectively. Energy dispersive spectroscopy (EDS) with four windowless detectors (SuperXG2) was used for composition analysis mapping.

WS_2 Growth. WS_2 was grown by hybrid metal organic chemical vapor deposition on a c-plane sapphire substrate with aqueous tungsten precursor and diethyl sulfide as sulfur precursor, as detailed in our previous work[24]. To prepare the aqueous tungsten precursor solution, 0.1 g potassium hydroxide and 0.6 g ammonium metatungstate were dissolved in 30 ml of deionized water. The c-plane sapphire substrate underwent an annealing process in an ambient environment at 1200 °C for 12 hours. The prepared aqueous tungsten precursor solution was then applied to the annealed substrate through a dip-coating method, followed by drying on a hot plate for 1 minute at 80 °C. The growth of WS_2 was completed by subjecting the dip-coated sapphire substrate to an annealing process at 775 °C for 6 hours. The annealing process involved a gas flow of 0.05 sccm diethyl sulfide, 1600 sccm Ar, and 1 sccm H_2. For this work, we used WS_2 bilayers grown in the uncoated area of the sapphire substrate.

(In Fig. 2, we also synthesized WS_2 bilayers on SiO_2/Si to study its roughness and Raman spectra directly after growth and/or NbP deposition, without the additional transfer step.)

Bilayer WS_2 Device Fabrication. WS_2 grown on sapphire was transferred onto 100 nm SiO_2/p^{++} Si with pre-patterned alignment marks. (We used the films grown on sapphire for devices because they displayed larger and more numerous bilayer regions than direct growth on SiO_2/Si.) The alignment marks were defined by lifting off 3 nm/12 nm Ti/Au. Polystyrene (PS) was spin-coated on top of the WS_2 on sapphire and then transferred in deionized water. PS was removed with toluene, and then a vacuum anneal (200 °C, 2 hours, ~10^{-6} Torr) was performed to promote adhesion. After the transfer, bilayer WS_2 triangles were identified using an optical microscope, and the alignment marks were used to place devices accurately onto them. Metal pads were patterned by electron-beam lithography (EBL), then 3 nm/20 nm Ti/Pt was electron-beam evaporated, and lifted-off. The channel was defined by EBL and then the WS_2 was dry etched using XeF_2. To define the fine contact region, a bilayer polymethyl methacrylate (PMMA) resist stack (PMMA 495K A2/PMMA 950K A2) was used. For the semimetal contact devices, ~3.5 nm of NbP (or TaP) was sputtered (see Methods: Semimetal Deposition), and then 10 nm/30 nm Pd/Au was immediately deposited by electron-beam evaporation at 0.5 Å/s at a base pressure of 10^{-8} Torr. We also fabricated control bilayer WS_2 devices with only Pd/Au (10/30 nm) contact metals. The control bilayer WS_2 devices were from the same growth as the semimetal-contacted devices and the Pd/Au contacts were evaporated in the same run as for NbP/Pd/Au and TaP/Pd/Au stacks to eliminate growth, transfer, and deposition variations.

Electrical Testing. Electrical measurements were performed at 296 K in a Janis ST-100 vacuum probe station at ~10^{-4} Torr, using a Keithley 4200 semiconductor parameter analyzer. Devices were not annealed in vacuum prior to measurement. To limit pad-to-substrate (back-gate) leakage, we monitored both drain and source current, ensuring they were in agreement. For the *p*-type doped samples, the devices were left in chloroform (>8 hours) and then re-measured in vacuum.

Bilayer WSe_2 Device Fabrication. Bilayer WSe_2 was grown on sapphire using solid-source CVD with solid Se and WO_3 as the precursors. 25 sccm Ar and 5 sccm H_2 were flowed as the carrier gases during the growth. The growth was conducted at 880 °C for 40 minutes at atmospheric pressure. The furnace was then cooled down to room temperature naturally. The WSe_2 material was then wet-transferred onto 100 nm SiO_2/p^{++} Si with pre-patterned alignment marks as described above. After the transfer, bilayer WSe_2 triangles were identified using an optical microscope, and the alignment marks were used to accurately place devices. Metal pads were patterned by electron-beam lithography (EBL), then 3 nm/20 nm Ti/Pt was electron-beam evaporated and lifted-off. The channel was defined by EBL and

then the WSe_2 was dry etched using XeF_2. To define the fine contact region, a bilayer polymethyl methacrylate (PMMA) resist stack (PMMA 495K A2/PMMA 950K A2) was used. NbP was deposited by RF-sputtering at room temperature at a power(voltage) of 9 W (36 V) for 15 minutes. The chamber pressure was kept below 5×10^{-8} Torr for the deposition. 10 nm/20 nm Pd/Au was electron-beam evaporated at 0.5 Å/s at a base pressure of 10^{-7} Torr. Liftoff of the metal stack was performed after soaking in acetone overnight, then rinsing in IPA. Prior to electrical testing, the WSe_2 devices were left in chloroform and then measured in vacuum at ~10^{-4} Torr at 296 K.

We used the transfer length method (TLM) to estimate the contact resistance, R_C (**Supplementary Fig. S11e**). The total resistance in a two-terminal device in kΩ·μm (normalized by the channel width) is $R_{TOT} = 2R_C + R_{sh}L$, where R_{sh} is the sheet resistance and L is the length of the channel. R_C is evaluated by plotting R_{TOT} versus L and the y-intercept at $L = 0$ gives the resultant $2R_C$. The R_C is extracted for each gate overdrive $|V_{GS} - V_T|$, with V_T from the constant-current method at $I_D = 10^{-2}$ μA/μm.

Density Functional Theory (DFT) Simulations. All DFT calculations were performed using Quantum ESPRESSO[51] (version 7.1) following a similar approach to that employed in a previous work[19]. First, we relax the appropriate super cell on a $15 \times 2 \times 1$ k-point grid until the force acting on each atom is less than 10^{-2} eV/Å in any direction. Afterwards, we perform self-consistent calculations on the relaxed structures on a $21 \times 3 \times 1$ k-point grid. We then perform a final non-self-consistent calculation on a $50 \times 7 \times 1$ k-point grid before extracting the projected density of states. For all calculations we use projector augmented wave pseudopotentials[53] with kinetic energy cutoffs of 70 Ry and charge density/potential cutoffs of 560 Ry; we model dispersion interactions using the DFT-D2 correction[54]; we truncate the potential in the out-of-plane direction using the method described in a previous work[55] using a large vacuum layer ≥ 5 nm; and we fix the unit cell to match the unit cell of WS_2 [i.e., x and y lattice vectors (see labels in **Fig. 5a**) of 22.04 and 3.18 Å for bilayer WS_2 and 21.89 and 3.16 Å for monolayer WS_2, respectively]. Electron occupations are described using Gaussian smearing using a spreading coefficient of 0.0025 Ry for structural relaxations. We used the tetrahedron method[56] for subsequent electronic structure calculations for all structures when extracting the density of states, except for the bilayer WS_2 contacts with tungsten (**Supplementary Fig. 12b,c**) which instead used Gaussian smearing (spreading coefficient of 0.0025 Ry).

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Author contributions. A.I.K. conceived the idea together with L.H. L.H. and A.I.K designed the experiments with input from E.P. A.I.K. formulated the semimetal contact deposition process on 2D TMD and optimized it with input from L.H. WS_2 growth was performed by Z.Z. and L.H. L.H. performed AFM and Raman characterization, fabricated the devices, and performed electrical measurements with input from E.P. and A.M. M.H. and L.H. performed and prepared samples for KPFM measurements. TEM and EDS characterization and analysis were performed by H-M.K. I-K.O. and A-R.C with input from A.I.K. R.K.A.B performed the simulations and relevant analysis with input from A.I.K and L.H. L.H., A.I.K., and R.K.A.B. wrote the manuscript together with E.P and A.M. All authors edited the manuscript. E.P. and A.M. supervised the work. **Competing interests.** A.I.K, L.H., R.K.A.B, E.P and A.M. are listed as co-inventors on a US patent provisional application (patent application number 63/572048) filed by The Board of Trustees of The Leland Stanford Junior University.

Data and materials availability: All data needed to evaluate the conclusions in this paper are present in the paper or the supplementary materials.

Supplementary Information

Supplementary Sections I and II

Figures S1 to S15

Table S1

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